Lecture 3:
Case Study in Electronic System Design

2015 Spring

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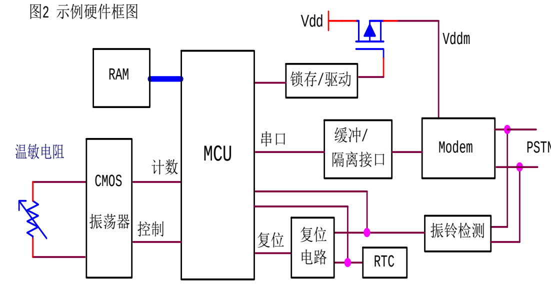
Outline

- **1. Overview**

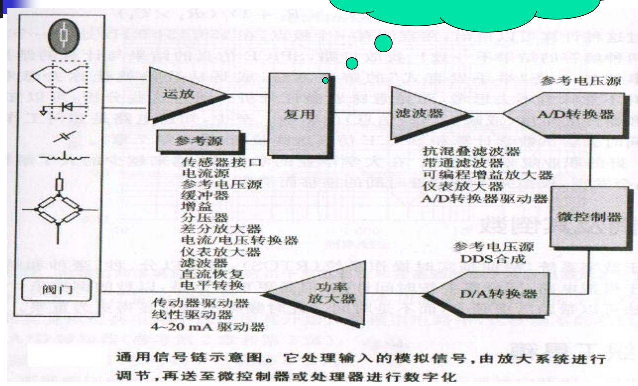
Electronic System based on MCU

图2 示例硬件框图



System Diagram
Signal Flow

Performance
(系统指标)



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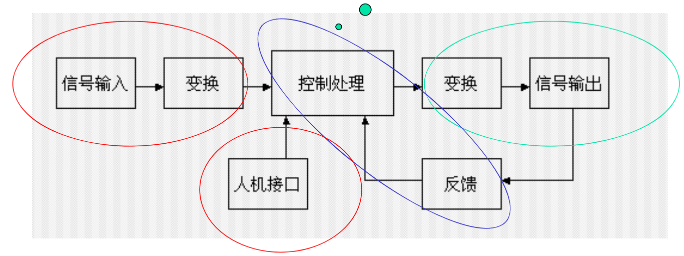
System Diagram
Logic Diagram

Performance
(系统指标)



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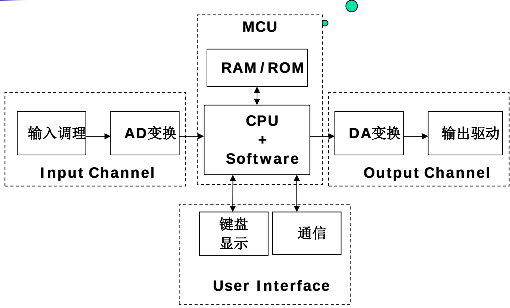
System Architecture

Performance
(系统指标)



- 2. Design Methodology

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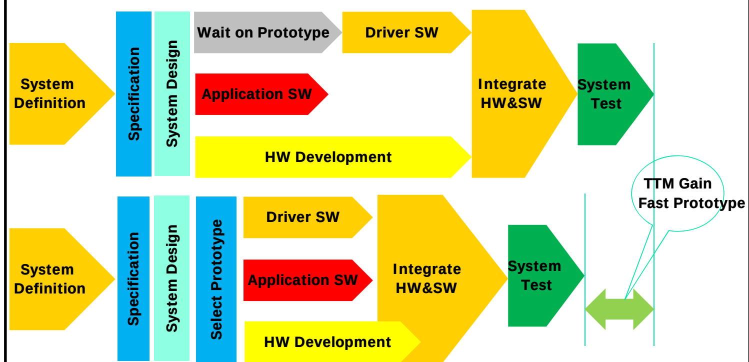
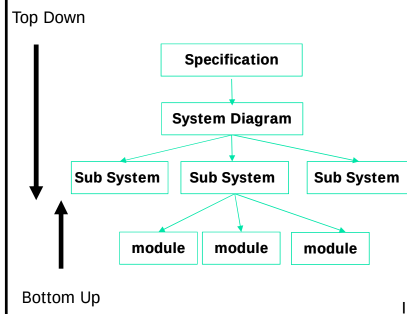
1.Design Flow

Traditional vs. Prototype based



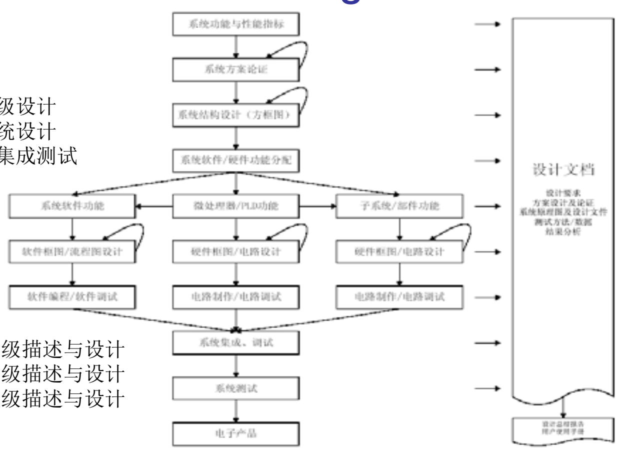
2. Top Down Methodology



- 功能要求
- 总体框图
- 子系统
- 单元电路
  - 选芯片
  - 原理图
  - 电路仿真
  - PCB图
  - 单元调试
- 系统调试
- 迭代反复

3.Process of Design

- 系统级设计
- 子系统设计
- 系统集成测试



- 行为级描述与设计
- 结构级描述与设计
- 物理级描述与设计

- 3. Case Study

3. Case Study: Digital Frequency Meter

- Case Study 1: System Requirement Analysis
- Case Study 2: System Design
- Case Study 3: Sub System Design
- Case Study 4: Software Design
- Case Study 5: System Test
- Case Study 6: Document

3.1 Case
1 Digital

- System Re

1．基本要求

（1）频率测量

a．测量范围 信号：方波、正弦波；幅度：0.5V～5V；频率：1Hz～1MHz

b．测量误差≤0.1%

（2）周期测量

a．测量范围 信号：方波、正弦波；幅度：0.5V～5V；频率：1Hz～1MHz

b．测量误差≤0.1%

（3）脉冲宽度测量

a．测量范围 信号：脉冲波；幅度：0.5V～5V；脉冲宽度≥100μs

b．测量误差≤1%

（4）显示器

十进制数字显示，显示刷新时间1～10秒连续可调，对上述三种测量功能分别用不同颜色的发光
示。

（5）具有自校功能，时标信号频率为1MHz。

（6）自行设计并制作满足本设计任务要求的稳压电源。

2．发挥部分

（1）扩展频率测量范围为0.1Hz～10MHz（信号幅度0.5V～5V），测量误差降低为0.01%（最大闸
≤10s）。

（2）测量并显示周期脉冲信号（幅度0.5V～5V、频率1Hz～1kHz）的占空比，占空比变化范围为
90%，测量误差≤1% 。

（3）在1Hz～1MHz范围内及测量误差≤1%的条件下，进行小信号的频率测量，提出并实现抗干扰

3.1 Case Study 1: System Requirement Analysis
2 Requirement Analysis

- Main Function
  - Frequency/Period/Pulse Width/Duty
- Main Specification
  - Duty Error<=1%, others Error <0.1%
  - Frequency Range:1Hz~10MHz
    - Advanced Function: 0.1Hz~10MHz
  - Pulse Width>=100us
  - Gate Time: 10s
  - Refresh Display: 1~10s
  - Input Level: 0.5~5V
    - Advanced :0.02V ~ 5V

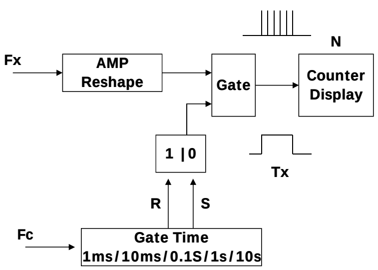
3.2 Case Study 2: System Design
1.Measure Principle Study

- Direct Algorithm
- Indirect Algorithm
- Multicycle Synchronization Algorithm

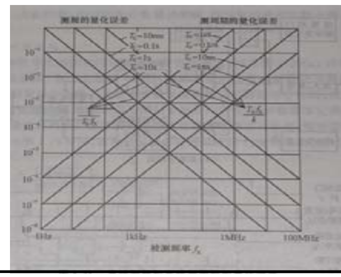
Duty Error<=1%, others Error <0.1%

3.2 Case Study 2: System Design
2. Direct Algorithm for Frequency

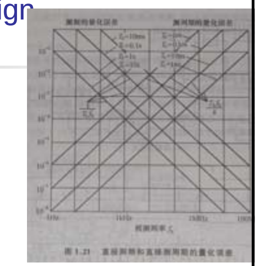
- Diagram



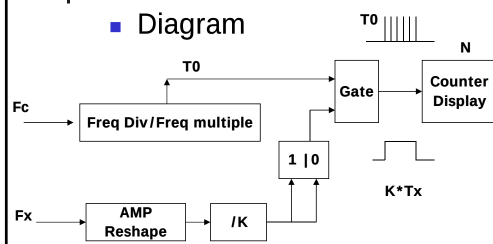
- Formula
  - Fx=N/Tx
  - ΔFx/Fx=(1/TsFx+| ΔFc/Fc|)



3.2 Case Study 2: System Design
3. Direct Algorithm for Period



- Diagram



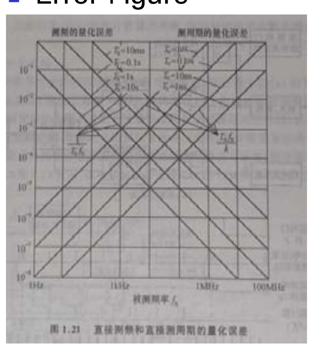
Trigger Error

- Formula
  - Tx = NT0/K
  - ΔTx/Tx=(T0Fx/K+| ΔFc/Fc|+0.32/K*Power(10,-SNR/20)

3.2 Case Study 2: System Design
4. Indirect Algorithm for Freq/Period

- Frequency → Period
- Period → Frequency
- Fm
  - Middle Frequency

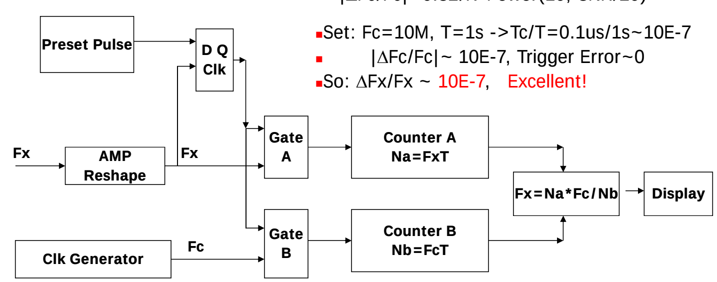
- Error Figure



3.2 Case Study 2: System Design
5. Multicycle Synchronization Algorithm

- Formula
  - Fx=Na*Fc/Nb
  - ΔFx/Fx= ΔTx/Tx=Tc/T+ |ΔFc/Fc|+0.32/K*Power(10,-SNR/20)
  - Set: Fc=10M, T=1s ->Tc/T=0.1us/1s~10E-7
  - |ΔFc/Fc|~ 10E-7, Trigger Error~0
  - So: ΔFx/Fx ~ 10E-7, Excellent!

- Diagram



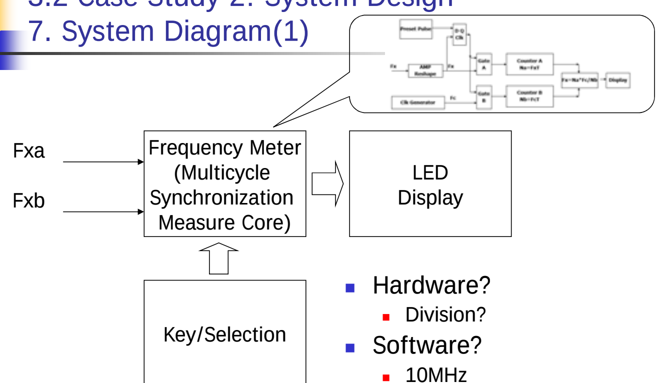
3.2 Case Study 2: System Design
6. Core Algorithm Selection

Algorithm	Error	Complex	Software Req.
Direct	×	Low	No
Indirect	Enough	Middle	Switch @ Fm Division
M.S	Good	Middle	Division

3.2 Case Study 2: System Design
6. Core Algorithm Double Check

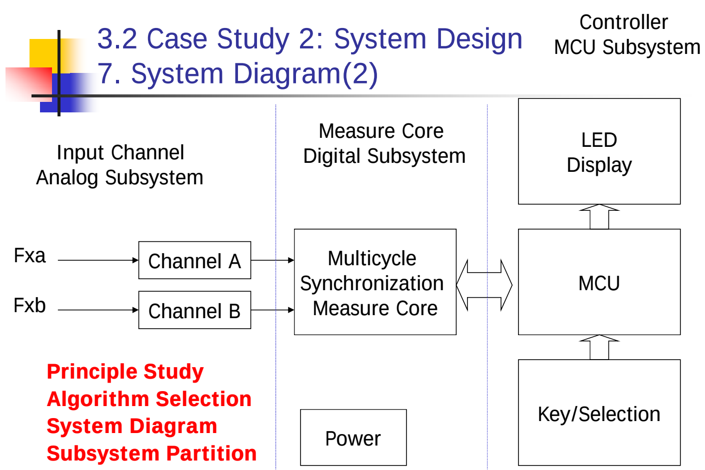
- Pulse Width
- Duty
- Advanced Requirement
- Other Specifications…

3.2 Case Study 2: System Design
7. System Diagram(1)



- Hardware?
  - Division?
- Software?
  - 10MHz
- Hardware/Software?
  - 10MHz/Division

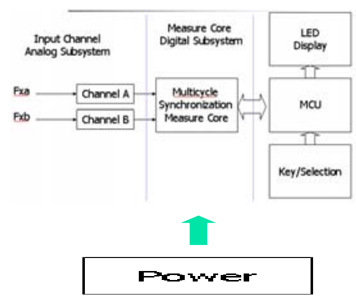
3.2 Case Study 2: System Design
7. System Diagram(2)



Principle Study
Algorithm Selection
System Diagram
Subsystem Partition

3.2 Case Study 2: System Design
7. System Diagram(3)

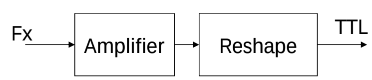
- Four Subsystems
  - Analog Subsystem
  - Digital Subsystem
  - MCU Subsystem
  - Power Subsystem



3.3 Case Study 3: Sub System Design(1)

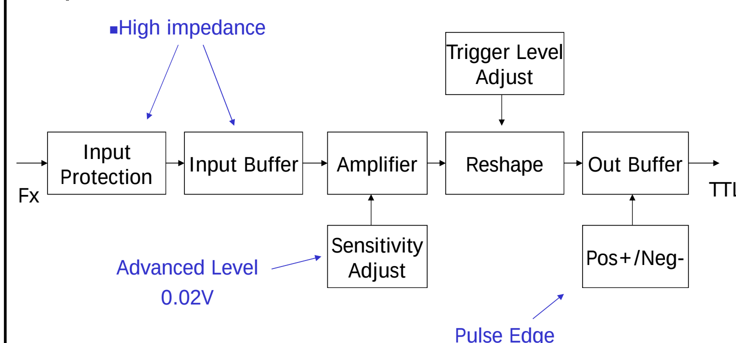
- **Analog Subsystem**
  - Input Channel

3.3 Case Study 3: Sub System Design(1)
1. Input Channel Requirement



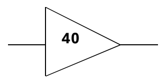
- Type
  - Analog Subsystem
- Requirement
  - Function
    - Convert Analog Signal to Digital Signal
  - Specification
    - Input signal
      - Level: 0.5V ~ 5V, Advanced: 0.02V~5V
      - Freq: 0.1Hz ~ 10MHz,
    - Output signal
      - Level: TTL
      - Freq: 0.1Hz ~10MHz

3.3 Case Study 3: Sub System Design(1)
2. Input Channel Diagram



3.3 Case Study 3: Sub System Design(1)
3. Input Channel : Amplifier + Reshape

- Reshape @ 0.02V input
  - TTL:
    - Trigger Level=2V
    - Gain = 2V/0.02V =100
  - Comparator
    - MAX902 , SR=0.5V/s
    - SR=2*Pi*Fx*Um → Um=0.8V @ Fx=0.1Hz
    - Gain = 0.8v/(0.02V* 1.414) = 30
    - Choose Gain=40 @ 0.02 input

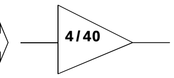


Reshape=Comparator

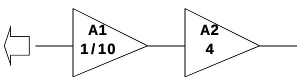
3.3 Case Study 3: Sub System Design(1)
4. Input Channel : Amplifier Double Check

- Amplifier
  - @5V Um= 40*5v*1.414 = 280V
  - @0.5V Um= 40*0.5*1.414 = 28V
  - @0.02VUm= 40*0.02*1.414 =1.2 V

- **Gain Switch**
  - **@0.5V~5V**
    - **Gain=4**
    - **Um=2.8V ~28V**
  - **@0.02V~0.5V**
    - **Set Gain =40**
    - **Um=1.2V~28V**



- GBW:GAIN*BW
  - 4* 10M = 40M
  - 40* 10M = 400M
    - **Too Large!**



- GBW=GAIN*BW
  - A1:
    - 1*10M=10M
    - 10*10M=100M
  - A2
    - 4*10M=40M

Max4016 + Max4016
GBW=150M

3.3 Case Study 3: Sub System Design(1)
5. Analog Subsystem Design Main Points

- Requirement Study & Analysis
- Module Partition & Specification Assignment
- Module Design
- Couple Circuit Design
- Specification Double Check

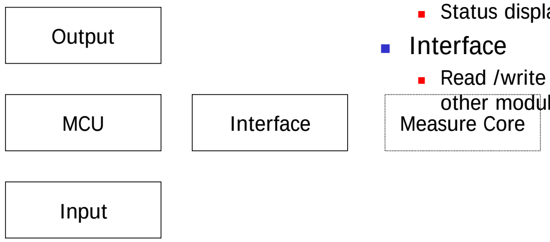
3.3 Case Study 3: Sub System Design(2)

- **MCU Sub System**

3.3 Case Study 3: Sub System Design(2)
1. Requirement for Controller

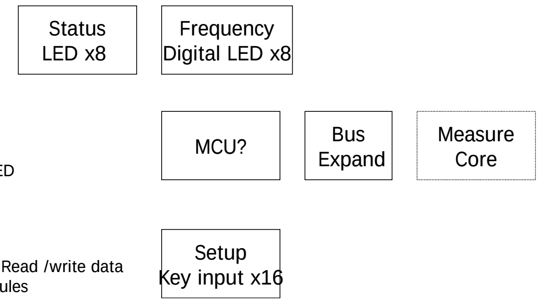
- Setup
- Display Frequency
- Control Measure Core

- Input:
  - KeyIn
- Output:
  - Digital display
  - Status display
- Interface
  - Read /write data with other modules



3.3 Case Study 3: Sub System Design(2)
2. MCU Sub system Diagram(1)

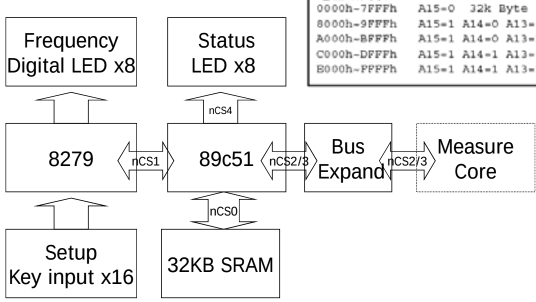
- Input:
  - Keyboard
    - 11 key
- Output:
  - Digital display
    - 8 Digital LED
  - Status display
    - 8 LED
- Expand
  - Parallel Bus for Read /write data with other modules

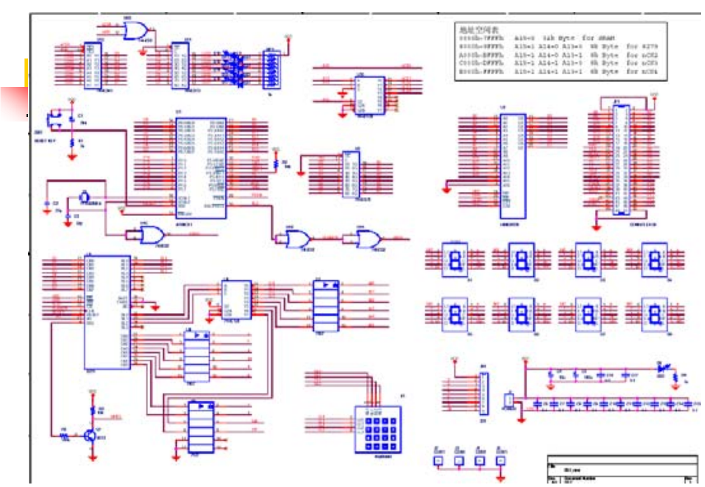


3.3 Case Study 3: Sub System Design(2)
3. MCU Sub system Diagram(2)

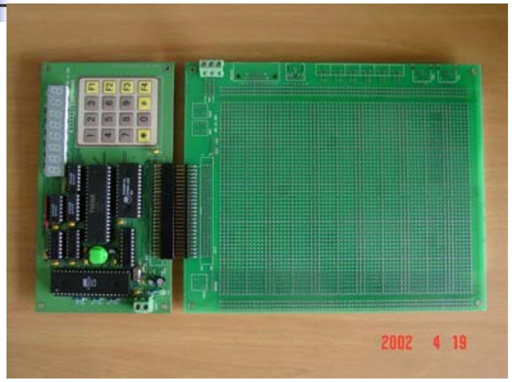
地址空间表

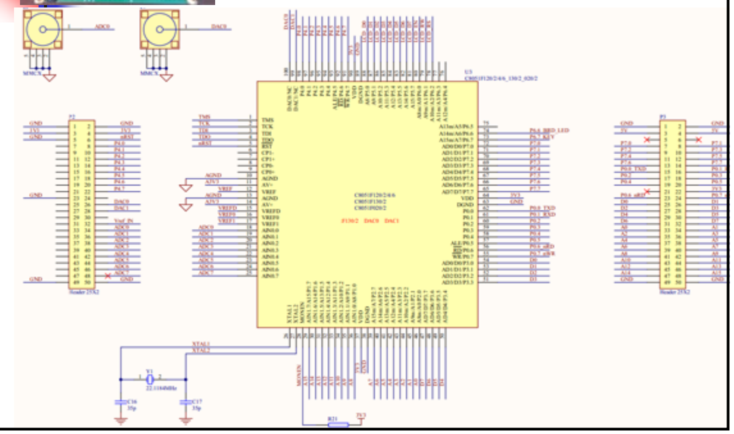
0000h-7FFFh	A15=0			32k Byte	for SRAM
8000h-9FFFh	A15=1	A14=0	A13=0	8k Byte	for 8279
A000h-BFFFh	A15=1	A14=0	A13=1	8k Byte	for nCS2
C000h-DFFFh	A15=1	A14=1	A13=0	8k Byte	for nCS3
B000h-FFFFh	A15=1	A14=1	A13=1	8k Byte	for nCS4





实物





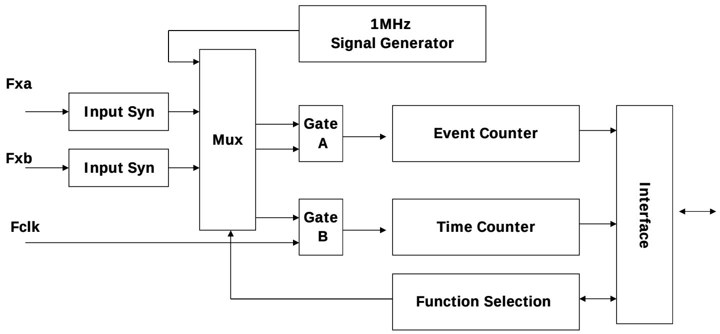
3.3 Case Study 3: Sub System Design(3)

- **Digital Sub System**
  - **Measure Core**

3.3 Case Study 3: Sub System Design(3)
1. Requirement for Measure Core

- Function
  - Multicycle Synchronization Measure Core
  - Measure Function Selection
    - Frequency,Period,Time
  - 1MHz Signal Generator
- Specification
  - Fclk =10MHz
  - Fx =10 MHz
  - Measure Precision

3.3 Case Study 3: Sub System Design(3)
2. Measure Core Diagram

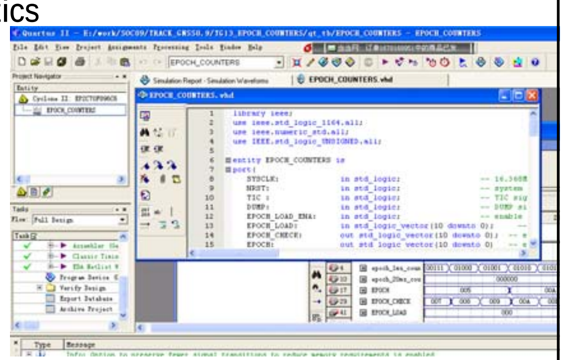


3.3 Case Study 3: Sub System Design(3)
3. Implementation Technology

	Speed	Flexibility	Debug	Capacity
MCU	Low	Good	Easy	Limit
MSI,SSI	Middle	Bad	Bad	Low
PLD	High	Good	Good	High

3.3 Case Study 3: Sub System Design(3)
4. Design Methodology

- Schematics
- VHDL
- Verilog



3.3 Case Study 3: Sub System Design(3)
5. Digital Subsystem Design Main Points

- Requirement Study & Analysis
- Subsystem Diagram
- Technology Selection
- Module Design/Debug
- Subsystem Debug

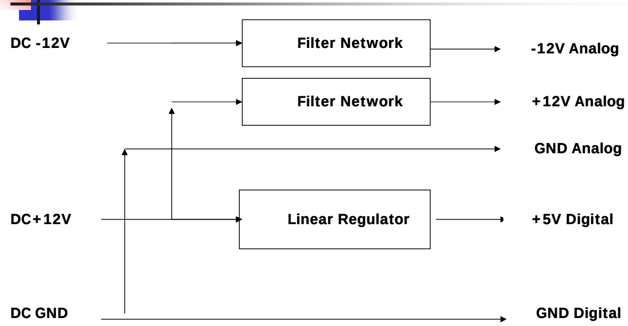
3.3 Case Study 3: Sub System Design(4)

- **Power Sub System**

3.3 Case Study 3: Sub System Design(4)
1. Requirement for Power Subsystem

- Functions
  - Inputs
    - DC/AC
  - Outputs
    - Analog/Digital/RF/Driving
  - Power Model
    - ON/OFF, Wake/Sleep/Battery
- Specifications
  - Voltage/Noise
  - Current/Max
- Design
  - Switch Power Supply
    - DC/DC,AC/DC
  - Linear Power Supply
    - LDO

3.3 Case Study 3: Sub System Design(4)
2. Power Subsystem Diagram



Double Check Maximum Current，>=150%

3.3 Case Study:Sub System Design
Summary

- Requirement Study & Analysis
- Algorithm Selection
- System Diagram
- Module Circuit Design
- Double Check

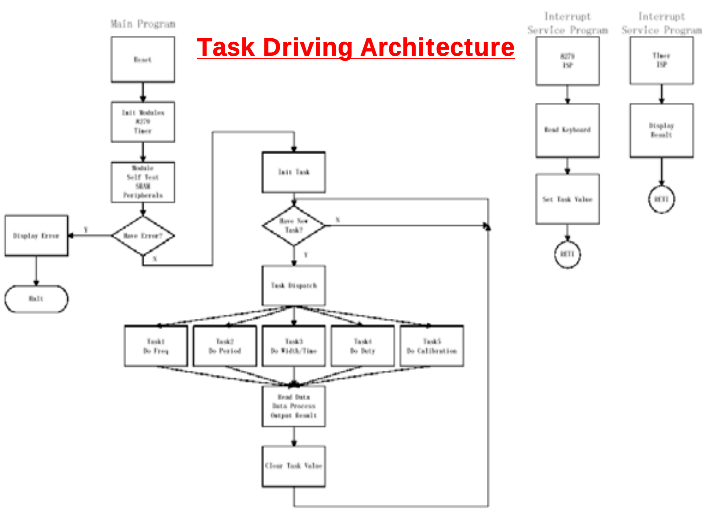
3.4 Case Study 4: Software Design
1. Requirement for Software Subsystem

- Function
  - Reset
  - Read Keyboard
  - Control the Measure Core
    - Freq,Period,Duty…
  - Read Measure Data
  - Data Process
  - Display Result

3.4 Case Study 4: Software Design
2.Diagram/Modules

- Modular Design
  - Main Program
    - **Reset**
    - **Init Modules/Self Test**
    - **Init Task**
    - **Task Dispatch**
  - Task Program
    - **Task1: Do Frequency**
    - **Task2: Do Period**
    - **Task3: Do Width/Time**
    - **Task4: Do Duty**
    - **Task5: Do Self Calibration**
  - Sub Program
    - **Read Data**
    - **Data Process**
    - **Output Result**
  - Interrupt Program
    - **Read Keyboard/Display Data**

Task Driving Architecture



3.4 Case Study 4: Software Design
4. MCU Software Design Main Points

- Requirement Study
- Task List
- Diagram/Modules
  - Main Program
  - Task Program
  - Public Sub Program
  - Interrupt Service Program
- System FlowChart
  - Task Driving Architecture
- Program/Debug
- Integrate

Coding Style

3.4 Case Study 4: Software Design
5. Fault-tolerant Design

- Reset
  - Flags to distinguish the reason
- Watch Dog
  - Hardware Counter
  - Software trigger
- Soft Trap
- Redundancy of Instruction
- Digital Filter:
  - Median Filter for AD data

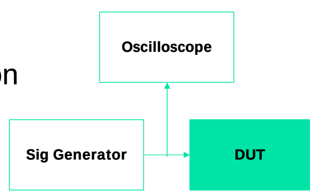
3.5.Case Study 5: System Test
1. Requirement

- System Test
  - Function
  - Specifications

- Functions
- Specifications

3.5 Case Study 5: System Test
2. System Test Plan

- Methodology
  - Test Configuration
  - Test Steps
- Instruments
  - Signal Generator
  - Oscilloscope



DUT: Device Under Test

3.5 Case Study 5: System Test
4. System Result

- Test Records
  - Data Set
    - Who/When/What
- Result
  - Conclusions
  - Analysis

- Functions
- Specifications

3.6 Case Study 6: Document
1.Requirement

（一）摘要
对本项目及完成情况的概要介绍，关键词。

（二）系统方案论证
对本项目采用的系统方案进行论证，要有多种方案的比较，给出所采用方案的系统框图。

（三）理论分析与计算
对本项目采用的部件（元器件）、方法、算法进行理论分析与计算，证明其符合要求。

（四）重要电路设计
对本项目采用的关键电路进行设计分析、比较，给出原理图。

（五）软件流程
软件流程图、模块说明。

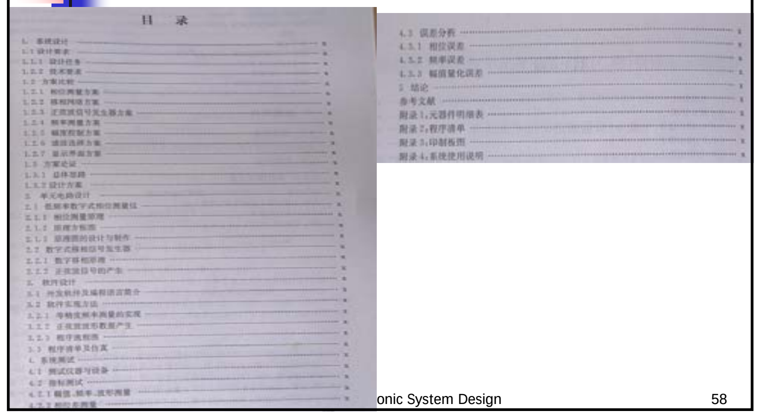
（六）系统功能及使用方法
类比使用说明书。

（七）系统测试及结果分析
给出测试方法、所使用仪器、测试数据及测试结果分析（误差分析）。

（八）进一步讨论
系统性能的进一步改进措施等。

（九）结束语

3.6 Case Study 6: Document
2.Example:低频数字式相位测量仪



- **4. Design Tips**

4. Design Tips
1.系统设计

- 可制造性设计（DFM）
  - 设计容差，边界条件和极限参数
  - 器件不同的封装、来源
- 可测试性设计(DFT)
  - 预先考虑调试，
    - Example: 预留测试点，闭环电路的开环断口
  - 可以自测试（Self-Test）
- 可扩展性设计
  - 基本+发挥
    - Example: 设计余量，接口

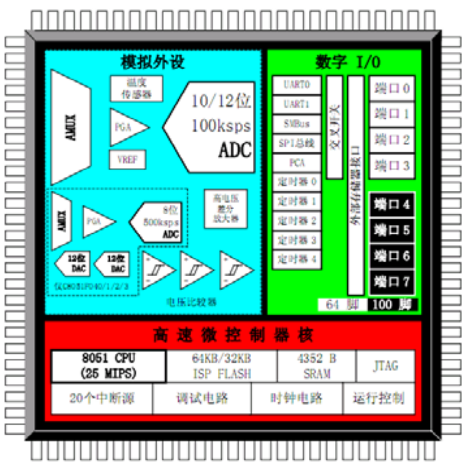
1.系统设计

- 模块化设计
  - 可替换，可单独调试
  - 功能单一
  - 连线简单
  - Example:
    - AD/DA 模块
    - 电源模块
    - 。。。

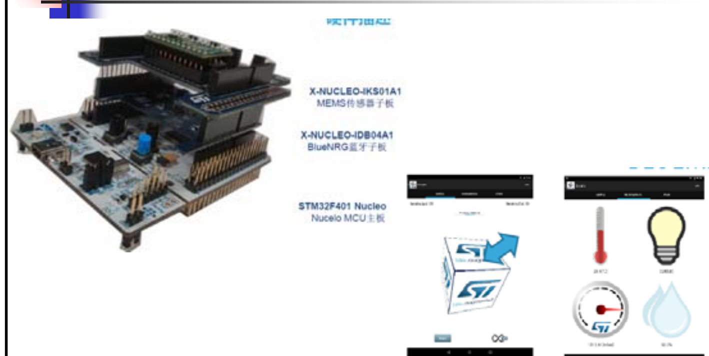
4. Design Tips
2. 新器件新技术的选择使用

- Example:
  - 单片机选用
    - 8051
      - Intel: 8031
      - Atmel: Flash+PW+WD
      - Philips: 33M+CAN+AD
      - CYGNAL: SOC: JTAG+8051+AD+温度
    - AVR: RISC+ ISP + C +Low Power+AD
    - PIC
    - Motorola 68H
    - Scenix单片机：50M
  - 工作温度范围
    - 民用级0℃~70℃，工业级是-40℃~85℃，军用级是-55℃~125℃

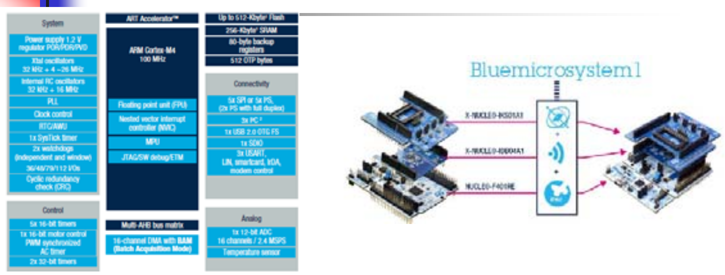
C8051F040



智能硬件口袋实验室 NucleoF401 套件



ARM-Cortex M 4 +低功耗蓝牙+MEMS传感器



- X-NUCLEO-IKS01A
  - LSM6DS0: MEMS 3D accelerometer (±2/±4/±8g) + 3D gyroscope (±245/±500/±2000 dps)
  - LIS3MDL: MEMS 3D magnetometer (±4/ ±8/ ±12/ 16 gauss)
  - LPS25HB*: MEMS pressure sensor, 260-1260 hPa absolute digital output barometer
  - HTS221: capacitive digital relative humidity and temperature

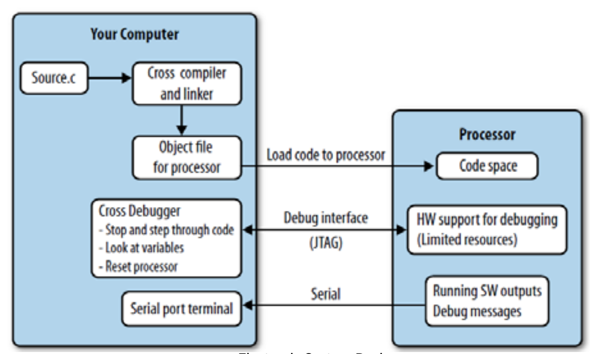
4.Design Tips
3. Debug Methodology

- 全局检查
  - 电源短路，接线错误
- 逐步调试
  - 逐级逐块安装，逐步调试

4.Design Tips
4. Analog Circuit Debug

- 晶体管电路
  - 检查工作点
  - 断开级联，断开反馈
- 运放
  - 差分输入端电位
  - 自激
  - 最好不要超过2级

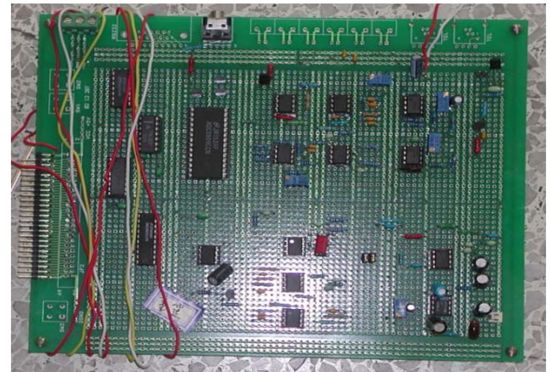
4.Design Tips
MCU debug: In Circuit Debug



4.Design Tips
5. PCB布线原则

- 布局均衡
- 电源线、地线尽可能粗
- 数字，模拟电路分开，地线不要混叠
- 低频一点接地，高频多点接地
- 电源滤波
  - 输入处接一个100uF电解电容
  - 每个集成电路电源接0.01uF小电容
  - 串接电感（铁氧芯）
- 相关器件靠近，接线短
- 散热要求

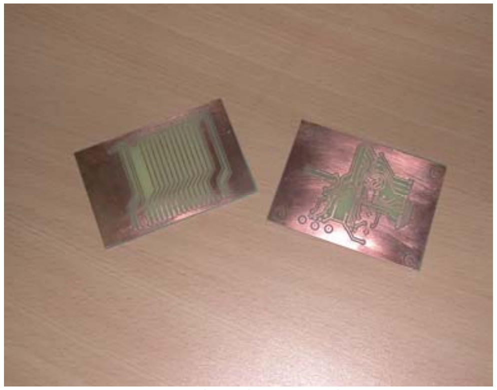
4.Design Tips
6. PCB布线原则：按信号流布局



PCB布线原则：
模拟与数字分区，电源滤波

PCB与外壳
接口匹配及安装定位

4.Design Tips
6. PCB布线原则：45度走线，地线覆盖

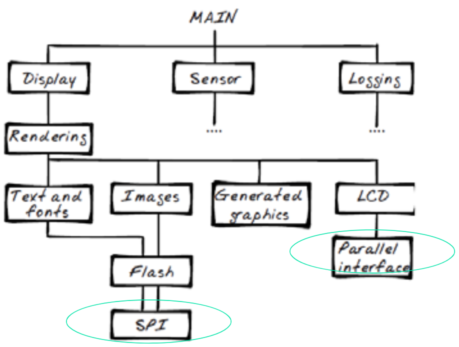


4.Design Tips
7. 可靠性测试

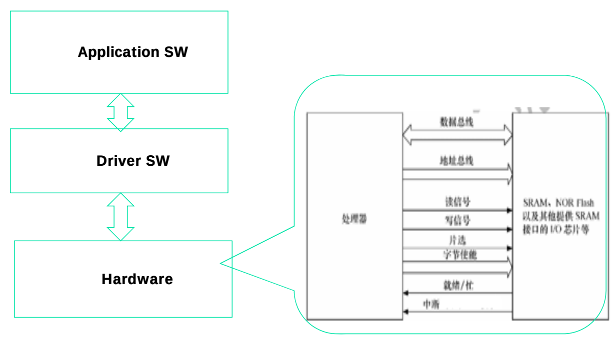
- 系统自测试
- 测试单片机软件功能的完善性
- 上电掉电测试
- 老化测试
- 电磁测试
  - 静电试验**(ESD)**
  - 空间辐射耐受试验**(RS)**
  - 快速脉冲抗扰测试**(EFT/B)**
  - 雷击试验**(Surge)**
  - 传导抗扰耐受性**(CS)**
  - 脉冲耦合（**Impulse**）

系统指标之一！！

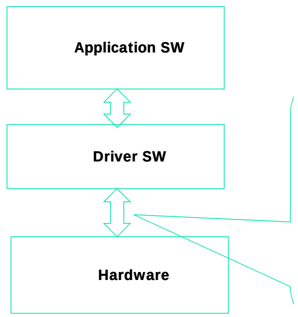
8.Program Model: Interface



Layer Model（No OS）

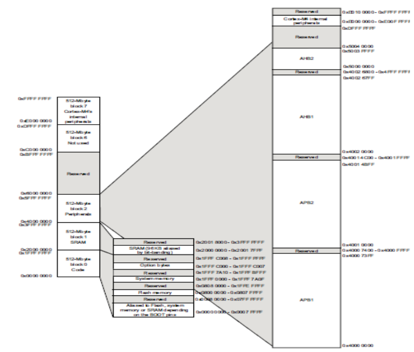


Layer Model（No OS） Memory Map Register

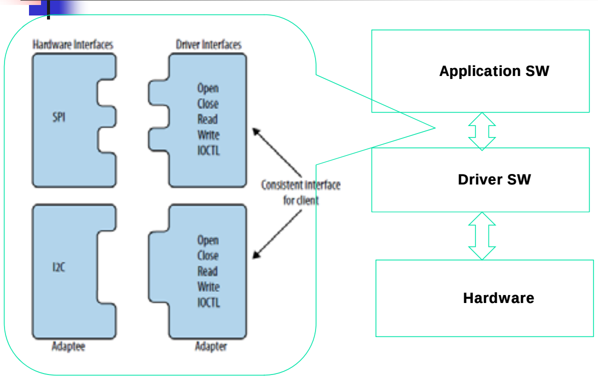


Bus	Boundary address	Peripheral
APB2	0x4001 4C00- 0x4001 FFFF	Reserved
	0x4001 4800 - 0x4001 4BFF	TIM11
	0x4001 4400 - 0x4001 47FF	TIM10
	0x4001 4000 - 0x4001 43FF	TIM9
	0x4001 3C00 - 0x4001 3FFF	EXTI
	0x4001 3800 - 0x4001 3BFF	SYSCFG
	0x4001 3400 - 0x4001 37FF	SPI4/I2S4
	0x4001 3000 - 0x4001 33FF	SPI1
	0x4001 2C00 - 0x4001 2FFF	SDIO
	0x4001 2400 - 0x4001 2BFF	Reserved
	0x4001 2000 - 0x4001 23FF	ADC1
	0x4001 1800 - 0x4001 1FFF	Reserved
	0x4001 1400 - 0x4001 17FF	USART6
	0x4001 1000 - 0x4001 13FF	USART1
	0x4001 0800 - 0x4001 0FFF	Reserved
	0x4001 0400 - 0x4001 07FF	TIM8
	0x4001 0000 - 0x4001 03FF	TIM1
	0x4000 7400 - 0x4000 FFFF	Reserved

STM32F401RE Bus → Memory Map Register



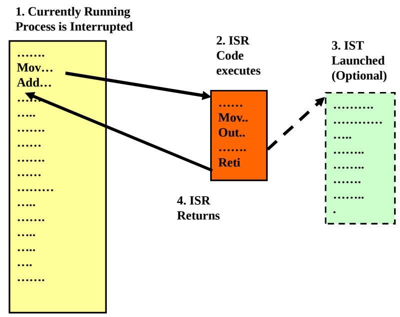
Program Model: Driver SW：SPI,I2C,UART



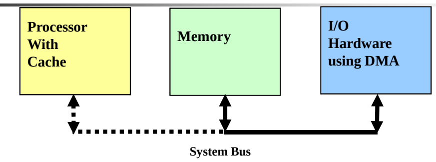
Program Model

- Memory Map Register
  - Read/Write
- Access Model
  - Software Polling
  - Interrupt
  - DMA

Servicing an Interrupt



DMA Bus Cycle



- Processor does not drive the bus during a DMA bus cycle
- Bus Arbitration hardware is needed to support multiple bus masters

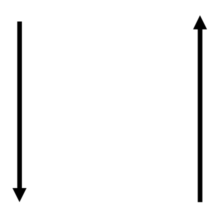
Tradeoffs

Transfer Technique ***Hardware*** ***CPU Overhead***

Programmed I/O

Interrupt

DMA

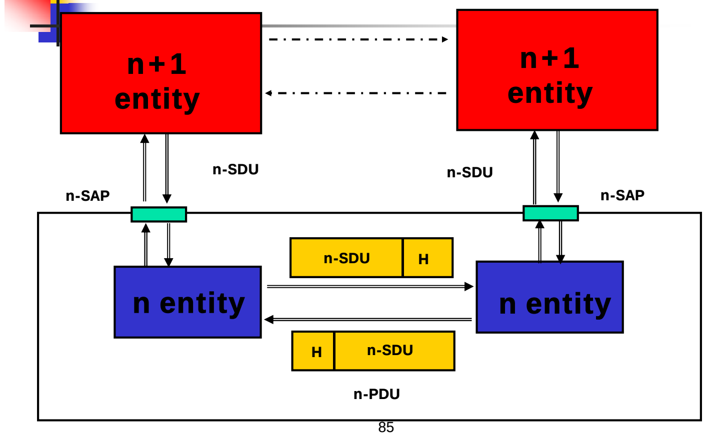


9.Program Model: Communication Software

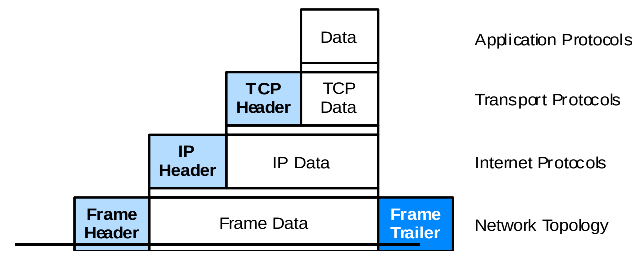
- 传输连接的建立和释放
- 差错控制
- 提供可靠透明的数据传输

- 指标：
  - **QOS**：吞吐量、延迟、安全

Layers, Services & Protocols



Network Protocol Layers



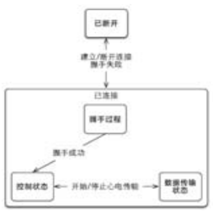
服务和协议的区别

- ❑ 服务是各层向它上层提供的一组原语（操作）
  - ❑服务定义了两层之间的接口
    - ❑上层是服务用户
    - ❑下层是服务提供者
  - ❑服务定义了该层能够代表它的上层完成的操作
  - ❑不涉及这些操作是如何完成的
- ❑ 协议是定义同层对等实体之间交换的帧、分组和报文的格式及意义的一组规则
  - ❑实体利用协议来实现它们的服务定义
  - ❑只要不改变提供给用户的服务，实体可以任意地改变它们的协议

协议需要实现的功能

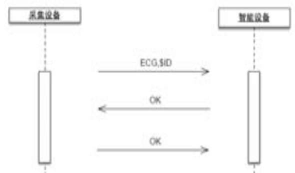
- 连接控制：连接/无连接
- 有序传送数据：不同路由，序号重排
- 流量控制：滑动窗控制
- 差错控制：检错/重发
- 分段/重装：协议报长限制
- 控制和数据封装：封装上层控制和数据
- 复用：多逻辑信道共用物理信道

Example:



步骤	方向	命令	描述
1	设备 → 手机	ECG,$ID\r\n	设备向手机发送设备类型(ECG)及 ID 号
2	手机 → 设备	OK\r\n(ERROR\r\n)	手机判断是否合法并给出反馈
3	设备 → 手机	OK\r\n	设备向手机确认

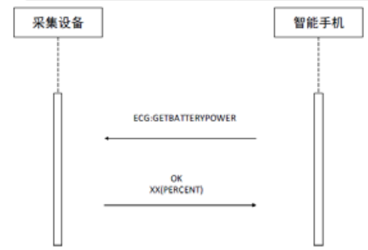
握手过程序列图如下所示



电量获取

卡片电量获取

描述	命令	成功响应	失败响应
获取电量	ECG:GETBATTERYPOWER \r\n	OK\r\n XX\r\n	ERROR\r\n



4.Design Tips
10. Reference Design resources

- Websites
  - www.21ic.com IC & Paper
  - www.icminer.com IC
  - www.zlgmcu.com 8051
  - www.altera.com.cn CPLD/FPGA
  - www.analog.com AD analog devices
  - www.maxim-ic.com.cn maxim IC
  - www.ti.com.cn TI IC

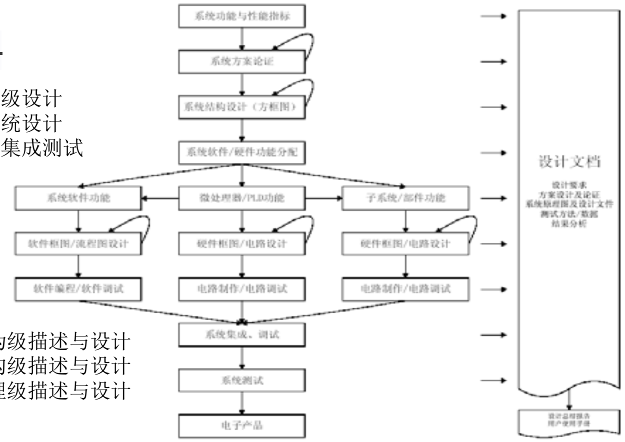
- **5. Summary**

5.Summary

- Today
  - Design Process
  - Case Study
- Important Points
  - Top→Down→Top
    - System→ Sub System → System
  - Three Design Levels
    - Behavior Design → Requirement
    - Structure Design → Diagram
    - Physical Implementation → Design
  - Modular Design
  - Design For Test

Process of Design

- 系统级设计
- 子系统设计
- 系统集成测试



- 行为级描述与设计
- 结构级描述与设计
- 物理级描述与设计

- Q/A?